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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/519,084	12/23/2004	Heiji Watanabe	Q85504	7332

23373 7590 04/15/2009

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EXAMINER	
CHIU, TSZ K	

ART UNIT	PAPER NUMBER
2822	

MAIL DATE	DELIVERY MODE
04/15/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/519,084	WATANABE ET AL.	
	Examiner	Art Unit	
	Tsz K. Chiu	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21-28,34-36 and 40* is/are allowed.

6)☒ Claim(s) *29-33 and 37-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 29-33 and 37-39 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 29-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamamoto (20020153579).

With respect to claim 29, Yamamoto discloses a semiconductor device a stacked gate insulating film (17 and 4, For example Fig. 5c) and a gate electrode (5b, For example Fig. 5c) stacked in this order on a silicon substrate (1, For example Fig. 5c) wherein

said gate insulating film (17 and 4, For example Fig. 5c) comprises a nitrogen (paragraph 27) containing high-dielectric-constant insulating film (4, For example Fig. 5c) which has a structure in which nitrogen (paragraph 27) is introduced into metal oxide (6, For example Fig. 5c) or metal silicate; and

a nitrogen (paragraph 27) atom in said nitrogen (paragraph 27) containing high-dielectric-constant insulating film (4, For example Fig. 5c) selectively bonds with a silicon atom in metal silicate.

With respect to claim 30, Yamamoto discloses a nitrogen (paragraph 27) atom which selectively bonds with a silicon atom in said metal silicate is situated at a distance from the silicon substrate (1, For example Fig. 5c).

With respect to claim 31, Yamamoto discloses, wherein said gate insulating film (17 and 4, For example Fig. 5c) comprises a silicon oxide film formed on said silicon substrate (1, For example Fig. 5c) so as to be in contact therewith, and said nitrogen (paragraph 27) containing high-dielectric-constant insulating film (4, For example Fig. 5c) formed on said silicon oxide film so as to be in contact therewith.

With respect to claim 32, Yamamoto discloses, wherein said silicon substrate (1, For example Fig. 5c) and said gate insulating film (17 and 4, For example Fig. 5c) are in contact with each other, and said gate insulating film (17 and 4, For example Fig. 5c) and a gate electrode (5b, For example Fig. 5c) are in contact with each other; and said gate electrode (5b, For example Fig. 5c) is made of either a polysilicon or a polysilicon germanium conductive film (paragraph 27).

With respect to claim 33, Yamamoto discloses the gate insulating film (17 and 4, For example Fig. 5c) contains at least one type selected from the group consisting of Zr, Hf, Ta, A1, Ti, Nb, Sc, Y, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb. Dy, Ho, Er, Tm, Yb and Lu (paragraph 76).

Claims 37-39 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al. (6844604).

With respect to claim 37, Lee discloses a semiconductor device stacked a gate insulating film (15, for example figure. 2) and a gate electrode (24, for example figure. 2) stacked in this order on a silicon substrate (10, for example figure. 2); wherein

said gate insulating film (15, for example figure. 2) has a layered structure having, from the silicon substrate side (10, for example figure. 2), a first silicon oxide film (column 8, lines 30-35), a metal oxide film or a metal silicate film (24, for example figure. 2) and a second silicon oxide film (column 8, lines 30-35); and

only the second silicon oxide film (column 8, lines 30-35) has a structure in which nitrogen is introduced into silicon oxide (column 4, lines 1-5).

With respect to claim 38, Lee discloses a semiconductor device according to Claim 21, wherein said silicon substrate (10, for example figure. 2) and said gate insulating film (15, for example figure. 2) are in contact with each other, and said gate insulating film (15, for example figure. 2) and a gate electrode (24, for example figure. 2) are in contact with each other; and said gate electrode is made of either a polysilicon or a polysilicon germanium conductive film (24, For example Fig. 2).

With respect to claim 39, Lee discloses the gate insulating film contains at least one type selected from the group consisting of Zr, Hf, Ta, A1, Ti, Nb, Sc, Y, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb. Dy, Ho, Er, Tm, Yb and Lu (column 8, lines 50-55).

Allowable Subject Matter

Claims 21-28, 34-36,40 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: Claim 21 is allowable over the reference of record because none of these references disclose or can be combined to yield the claimed invention of a semiconductor device stacked a gate with gate insulating film comprises a nitrogen containing high-dielectric-constant insulating film a position at which the nitrogen concentration in said nitrogen containing high-dielectric-constant insulating film reaches a maximum in the direction of the film thickness is present in a region at a distance from the silicon substrate.

Claim 34 is allowable over the reference of record because none of these references disclose or can be combined to yield the claimed invention of a semiconductor device stacked a gate with gate insulating film comprises a nitrogen containing high-dielectric-constant insulating film nitrogen is introduced only into a region lying between the position at which the silicon concentration has the minimum value and said gate electrode side interface.

Claim 40 is allowable over the reference of record because none of these references disclose or can be combined to yield the claimed invention of a semiconductor device stacked a gate with gate insulating film comprises a nitrogen containing high-dielectric-constant insulating film a position at which the nitrogen concentration in said gate insulating film reaches a maximum in the direction of the film thickness is present in a region at a distance from the silicon substrate.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tsz K. Chiu whose telephone number is 571-272-8656. The examiner can normally be reached on 0800 to 1700.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra V. Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Zandra V. Smith/
Supervisory Patent Examiner, Art Unit 2822

TC
April 12, 2009